Notice of Allowability	Application No.	Applicant(s)	
	10/029,520	HEMKER ET AL.	
	Examiner	Art Unit	
	Alexander Markoff	1746	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 11/28/05 and interviews conducted on 12/2/05 and 12/5/05*.

2. ☒ The allowed claim(s) is/are *1-11,14,21 and 22*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Paul Link on 12/5/05.

The application has been amended as follows:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for backside particle removal, comprising the operations of:

~~defining~~ identifying ~~cleaning~~ contact sites on a backside of a wafer, wherein the contact ~~cleaning~~ sites are portions of the backside of the wafer that physically contact a surface of a chuck having a predefined shape, the physical contact occurring when the backside of the wafer is placed in physical contact with the predefined shape of the surface during a semiconductor fabrication process; and

cleaning the ~~cleaning~~ contact sites on the backside of the wafer, the cleaning omitting cleaning of the portions of the backside of the wafer not having physical contact with the predefined shape of the surface of the chuck during the semiconductor fabrication process.

2. (Currently Amended) A method as recited in claim 1, further comprising the operation of aligning the ~~cleaning~~ contact sites with the predefined shape of the surface ~~contact regions~~ of the chuck after the cleaning of the ~~cleaning~~ contact sites in preparation for the semiconductor fabrication process, wherein the predefined shape of the surface ~~contact regions are regions~~ of the chuck ~~that~~ physically contacts ~~contact~~ the backside of the wafer during the semiconductor fabrication process.

3. (Previously presented) A method as recited in claim 2, wherein the chuck includes a chuck pin array, wherein the contact regions correspond to pin positions of the chuck pin array.

4. (Previously presented) A method as recited in claim 2, wherein the chuck is a vacuum chuck, and the contact regions correspond to wafer contact areas on the vacuum chuck.

5. (Currently Amended) A method as recited in claim 1, further comprising the operation of pre-programming the contact ~~regions~~ sites into a cleaning controller.

6. (Currently Amended) A method as recited in claim 1, wherein a laser is utilized to clean the contact sites on the backside of the wafer.

7. (Currently Amended) A method as recited in claim 1, wherein a megasonic wand is utilized to clean the contact sites on the backside of the wafer.

8. (Currently Amended) A system for backside particle removal, comprising:

a cleaning controller ~~that defines cleaning~~ programmed to identify contact sites on a backside of a wafer, wherein the ~~cleaning~~ contact sites are portions of the backside of the wafer that physically contact a surface of a chuck having a predefined shape, the physical contact occurring when the backside of the wafer is placed in physical contact with the predefined shape of the surface during a semiconductor fabrication process and programmed to omit cleaning portions of the backside of the wafer not having physical contact with the predefined shape of the surface of the chuck during the semiconductor fabrication process; and

~~an~~ a site specific cleaning apparatus ~~configured~~ controlled by the cleaning controller to clean the ~~cleaning~~ contact sites on the backside of the wafer defined by the cleaning controller, where the ~~clean~~ site specific cleaning apparatus omits cleaning portions of the backside of the wafer not having physical contact with the predefined shape of the surface of the chuck during the semiconductor fabrication process.

9. (Currently Amended) A system as recited in claim 8, further comprising a wafer aligning apparatus that aligns the ~~cleaning~~ contact sites with the predefined shape of the surface ~~contact regions~~ of the chuck, wherein the ~~contact regions are regions~~ predefined shape of the surface of the chuck ~~that~~ physically ~~contact~~ contacts the backside of the wafer during the semiconductor fabrication process.

10. (Currently Amended) A system as recited in claim 9, wherein the chuck includes a pin array that supports the wafer, and wherein the contact ~~regions~~ sites correspond to pin positions of the pin array.

11. (Currently Amended) A system as recited in claim 9, wherein the chuck includes grooves for applying a vacuum to the backside of the wafer, and wherein the contact ~~regions~~ sites correspond to areas of the chuck outside the grooves.

12. (Canceled)

13. (Canceled)

14. (Currently Amended) A system as recited in claim 8, wherein the site specific cleaning apparatus is integrated with a lithographic stepper apparatus.

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Currently Amended) A system for backside particle removal, comprising:

a cleaning controller ~~that defines cleaning~~ programmed to identify contact sites on a backside of a wafer, wherein the ~~cleaning~~ contact sites are portions of the backside of the wafer that physically contact a surface of a chuck having a predefined shape, the physical contact occurring when the backside of the wafer is placed in physical contact with the predefined shape of the surface during a semiconductor fabrication process and programmed to omit cleaning portions of the backside of the wafer not having physical contact with the predefined shape of the surface of the chuck during the semiconductor fabrication process; and

a megasonic wand controlled by the cleaning controller to clean the ~~cleaning~~ contact sites on the backside of the wafer defined by the cleaning controller, wherein the ~~clean~~ megasonic wand omits cleaning portions of the backside of the wafer not having physical contact with the predefined shape of the surface of the chuck during the semiconductor fabrication process.

22. (Currently Amended) A system for backside particle removal, comprising:

a cleaning controller ~~that defines cleaning~~ programmed to identify contact sites on a backside of a wafer, wherein the ~~cleaning~~ contact sites are portions of the backside of the wafer that physically contact a surface of a chuck having a predefined shape, the physical contact occurring when the backside of the wafer is placed in physical contact with the predefined shape of the surface during a semiconductor fabrication process and programmed to omit cleaning portions of the backside of the wafer not having physical contact with the predefined shape of the surface of the chuck during the semiconductor fabrication process; and

a laser controlled by the cleaning controller to clean the ~~cleaning~~ contact sites on the backside of the wafer defined by the cleaning controller, wherein the ~~clean~~ laser omits cleaning portions of the backside of the wafer not having physical contact with the predefined shape of the surface of the chuck during the semiconductor fabrication process.

23. (Canceled)

2. The following is an examiner's statement of reasons for allowance: the claims as amended directed to a method and apparatus, which comprise steps/means for identification of the contact sites on the wafer, wherein the contact sites are portions of the backside of the wafer that physically contact a surface of a chuck having a predefined shape, the physical contact occurring when the backside of the wafer is placed in physical contact with the predefined shape of the surface during a semiconductor fabrication process and step/means for cleaning the contact sites on the backside of the wafer, the cleaning omitting cleaning of the portions of the backside of the wafer not having physical contact with the predefined shape of the surface of the chuck during the semiconductor fabrication process. The prior art fails to teach or fairly suggest such method/apparatus. The prior art teaches cleaning of the entire wafer surface or cleaning all the areas wherein the contaminants are detected. No teaching or suggestions to clean only contacts sites and not to clean all other areas of the wafer wherein the contaminants are presented is found in the prior art.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Markoff whose telephone number is 571-272-1304. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Barr can be reached on 571-272-1414. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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AM

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